57. (New) A multibank memory device allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:

a plurality of memory banks, each memory bank including a plurality of memory cores arranged in strips of rows and columns;

a plurality of sense amplifiers shared among the memory cores of different ones of the plurality of memory banks;

a plurality of column decoders, each column decoder exclusively accessing a row of memory cores from only two of the plurality of memory banks wherein the memory cores are separated from each other in the strip by shared sense amplifiers whereby the memory cores of the strip alternate between the two memory banks.

58. (New) A memory architecture having n banks of memory banks which allows simultaneous access of some of the memory banks, comprising a plurality of memory banks, each memory bank including a plurality of memory cores arranged in rows, each row having an associated column decoder connected to each memory core of the row and each core of the row associated with only one of two memory banks.

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59. (New) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks while suffering reduced noise in sense amplifiers, comprising:

a plurality of memory banks, each memory bank containing a plurality of memory cores arranged in strips, each strip containing two memory banks and the strip having cores arranged to be alternating between the two memory banks with sense amplifiers shared between the cores of the two memory banks.

60. (New) A multibank memory architecture allowing simultaneous access of some of a plurality of memory banks comprising a row of memory cores interspersed between shared sense amplifiers, each memory core being a part of one of N memory banks, the strip having the